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09/051,263	08/07/1998	GEORGE W. SHAW	0081-012	7818

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
11/16/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/051,263	SHAW ET AL.	
	Examiner	**Art Unit**	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _07 September 2010_.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _45-62 and 77-85_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _45-62 and 77-85_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _29 June 2007_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 45-62 and 77-85 have been considered. Claims 77 and 84-85 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 07 September 2010.

Response to Arguments

3. Applicant's arguments filed 07 September 2010 have been fully considered but they are not persuasive.

4. Applicants' argue in essence on pages 8-9 "...Hanafi et al. is <u>not</u> ' a CMOS oscillator,' as recited...". This has not been found persuasive. While the CMOS driver, which produces the oscillating waveforms shown in Figure 2 and Figure 11(b), was developed to reduce noise in chip-to-chip communication, the reasons for designing and developing a device does not preclude the device from being used in other situations, Such as driving an oscillating signal used for a clock. Hanafi shows examples of oscillating output from its CMOS driver in Figure 2 and Figure 11(b). As stated in the previous rejection, copied below, Miller teaches an oscillating clock signal, but does not explicitly stated what drives the oscillating clock signal. Hanafi teach a CMOS driver circuit driving oscillating signals.

5. Applicants' argue in essence on page 9, "…it appears that the signal driver/receiver of Hanafi et al. is <u>not</u> located off of its respective chip in the multichip system…". This has not been found persuasive. Hanafi shows in Figure 7 a chip ground not connected to the driver and shows the line around the chip logic and pre-driver chip elements to an "on-chip decoupling". If

the driver was on-chip, it would be included along with the other elements connected to "on-chip decoupling" and on-chip ground, so that it would be decoupled and grounded with other on-chip elements. As it is, Figure 7 shows the driver as a separate entity from the other elements that are definitely marked as on-chip. Also, the cited paragraphs merely indicate that noise coming from off-chip comes from the L1 and L2 lines. This does not indicate that the driver is not off-chip.

6. Applicants' argue in essence on pages 10-11, "…none of these elements appear to be a programmable interface." This has not been found persuasive. A programmable interface is simply an interface that responds to program instructions. Anything in Miller's Figure 2 that interfaces with memory or other storage in response to program instructions, i.e. it's programmable, is a programmable memory interface. For example, the CPU accesses, i.e. interfaces, memory in response to program instructions.

7. Applicants' request on page 12 "Constructive Assistance from the Examiner". The Examiner encourages Applicants' or Applicants' representative to contact the examiner to schedule an interview to achieve this.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 45, 54-62, 77-78, and 83-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent Number 4,292,668 (herein referred to as Miller) in

view of Hanafi et al.'s "Design and Characterization of a CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance" IEEE ©1992 (herein referred to as Hanafi).

10. Referring to claim 45, Miller has taught a microprocessor system, comprising:

a. a microprocessing unit (MPU) (Miller Abstract; column 1, line 60 to column 2, line 2; column 13, lines 14-45; column 14, lines 26-57; Figure 1; and Figure 3);

b. an input-output processor (IOP) (Miller Abstract; column 2, line 29 to column 3, line 13; column 13, lines 14-45; column 14, lines 26-57; Figure 1; and Figure 3);

c. a global memory unit coupled to said MPU and to said IOP (Miller column 3, line 16 to column 4, line 12; column 16, lines 36-54; Figure 1; and Figure 2);

d. a direct memory access controller (DMAC) (Miller column 5, line 64 to column 8, line 10; column 14, lines 26-57; column 31, line 28 to column 32, line 46; Figure 1; and Figure 3);

e. an interrupt controller (INTC) (Miller column 33, line 51 to column 34, line 43 and Figure 23);

f. a programmable memory interface (MIF) (Miller column 17, line 30 to column 18, line 15 and Figure 2);

g. an oscillator, operating in conjunction with a clock multiplier (Miller column 24, line 35 to column 26, line 35);

h. a plurality of bit inputs (Miller column 13, line 16 to column 14, line 23; column 16, line 56 to column 17, line 68; Figure 1; Figure 2; and Figure 5); and

i. a plurality of bit outputs (Miller column 13, line 16 to column 14, line 23; column 16, line 56 to column 17, line 68; Figure 1; Figure 2; and Figure 5).

11. Miller has not explicitly taught the oscillator is a CMOS oscillator. However, Miller has taught the oscillator drives the internal clock (Miller column 24, line 35 to column 26, line 35). Hanafi has taught a CMOS signal driver (Hanafi Abstract). A person of ordinary skill in the art at the time the invention was made would have recognized that the CMOS signal driver reduces signal noise without delaying the signal (Hanafi Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hanafi's CMOS signal driver into the device of Miller to reduce signal noise without delaying the signal.

12. Referring to claim 54, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said MPU comprises a plurality of global data registers and a plurality of local registers (Miller column 15, line 50 to column 16, line 34 and Figure 4).

13. Referring to claim 55, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said global memory unit is shared by said MPU, said IOP, and said MIF (Miller column 3, line 16 to column 4, line 12; column 16, lines 36-54; Figure 1; and Figure 2).

14. Referring to claim 56, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said global memory unit is used for data storage and control communication with said DMAC and said IOP (Miller Abstract; column 2, line 29 to column 3, line 13; column 3, line 16 to column 4, line 12; column 16, lines 36-54; column 5, line 64 to column 8, line 10; column 13, lines 14-45; column 14, lines 26-57; column 31, line 28 to column 32, line 46; Figure 1; Figure 2; and Figure 3).

15. Referring to claim 57, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said global memory unit is used by said IOP for transfer information, loop

counts, and delay counts (Miller Abstract; column 2, line 29 to column 3, line 13; column 3, line 16 to column 4, line 12; column 16, lines 36-54; column 5, line 64 to column 8, line 10; column 13, lines 14-45; column 14, lines 26-57; column 31, line 28 to column 32, line 46; Figure 1; Figure 2; and Figure 3).

16. Referring to claim 58, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said MIF is shared by said IOP, said MPU, said DMAC, said plurality of bit outputs, and said plurality of bit inputs (Miller column 17, line 30 to column 18, line 15 and Figure 2).

17. Referring to claim 59, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: bus transaction requests are arbitrated and prioritized by said MIF (Miller column 17, line 30 to column 18, line 15 and Figure 2).

18. Referring to claim 60, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said INTC is shared by said plurality of bit inputs, said IOP, and said DMAC (Miller column 33, line 51 to column 34, line 43 and Figure 23).

19. Referring to claim 61, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein: said global memory unit comprise a plurality of registers (Miller column 15, line 50 to column 16, line 34 and Figure 4).

20. Referring to claim 62, Miller in view of Hanafi has taught the microprocessor system of claim 61, wherein: said plurality of global registers are used for operand storage for said MPU, and for data storage for said IOP (Miller column 15, line 50 to column 16, line 34 and Figure 4).

21. Referring to claim 77, Miller in view of Hanafi has taught the microprocessor system of claim 45, wherein:

a. at least said MPU (Miller Abstract; column 1, line 60 to column 2, line 2; column 13, lines 14-45; column 14, lines 26-57; Figure 1; and Figure 3), said IOP (Miller Abstract; column 2, line 29 to column 3, line 13; column 13, lines 14-45; column 14, lines 26-57; Figure 1; and Figure 3), and said MIF are located on-chip (Miller column 17, line 30 to column 18, line 15 and Figure 2); and

b. said CMOS oscillator is located off-chip (Hanafi Abstract).

22. Referring to claim 78, Miller in view of Hanafi has taught the microprocessor system of claim 77, wherein said clock multiplier is located on-chip (Miller column 24, line 35 to column 26, line 35).

23. Referring to claim 83, Miller in view of Hanafi has taught the microprocessor system of claim 45, further comprising:

a. a bus utilized by at least said MPU and said IOP (Miller column 17, line 30 to column 18, line 15 and Figure 2); and wherein

b. said MIF is operative to arbitrate and prioritize a plurality of bus transaction requests generated by said MPU and said IOP, said bus transaction requests associated with said bus (Miller column 17, line 30 to column 18, line 15 and Figure 2).

24. Referring to claim 84, Miller in view of Hanafi has taught the microprocessor system of claim 83, wherein: said MIF gives priority to said bus transaction requests generated by said IOP over said bus transaction requests generated by said MPU (Miller column 17, line 30 to column 18, line 15 and Figure 2).

25. Referring to claim 85, Miller in view of Hanafi has taught the microprocessor system of claim 83, wherein:

a. said bus is further utilized by said DMAC (Miller column 17, line 30 to column 18, line 15 and Figure 2); and

b. said MIF is further operative to arbitrate and prioritize said bus transaction requests generated by said MPU, said IOP, and said DMAC (Miller column 17, line 30 to column 18, line 15 and Figure 2).

26. Claims 46-47 and 79-80 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Hanafi as applied to claim 45 above, and further in view of Craft, U.S. Patent Number 4,321,706 (herein referred to as Craft). Miller has not explicitly taught

a. The microprocessor system of claim 45, wherein: a frequency of said oscillator is doubled internally to operate said MPU and said IOP (Applicants' claim 46).

b. The microprocessor system of claim 45, wherein: said microprocessor system utilizes a phase locked loop circuit (Applicants' claim 47).

27. Craft has taught

a. The microprocessor system of claim 45, wherein: a frequency of said oscillator is doubled internally to operate said MPU and said IOP (Applicants' claim 46) (Craft Abstract and column 4, line 66 to column 5, line 24).

b. The microprocessor system of claim 45, wherein: said microprocessor system utilizes a phase locked loop circuit (Applicants' claim 47) (Craft Abstract and column 4, line 66 to column 5, line 24).

28. A person of ordinary skill in the art at the time the invention was made, and as taught by Craft, would have recognized that the phase locked loop circuit with the specific oscillator frequency increases accuracy, lowers noise, and increases reliability (Craft column 4, lines 36-64). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to improve accuracy, lower noise, and increase reliability.

29. Referring to claim 79, Miller in view of Hanafi and in further view of Craft has taught the microprocessor system of claim 77, wherein: said clock multiplier includes at least one phase locked loop circuit (Craft Abstract and column 4, line 66 to column 5, line 24).

30. Referring to claim 80, Miller in view of Hanafi and in further view of Craft has taught the microprocessor system of claim 77, wherein

a. a frequency of said oscillator is quadrupled internally (Craft Abstract and column 4, line 66 to column 5, line 24); and

b. said quadrupled frequency is used by said MIF (Miller column 17, line 30 to column 18, line 15; Figure 2; column 24, line 35 to column 26, line 35).

31. Claims 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Hanafi as applied to claim 45 above, and further in view of Official Notice.

32. Referring to claim 48, Miller in view of Hanafi has not taught the microprocessor system of claim 45, wherein: said MPU retrieves up to four instructions from memory for each instruction fetch or prefetch. Official Notice is taken on this limitation. A person of ordinary skill in the art at the time the invention was made would have recognized that increasing the number of instructions fetched improves processor efficiency, since it decreases the amount of time needed to fetch instructions.

33. Referring to claim 49, Miller in view of Hanafi has not taught the microprocessor system of claim 45, wherein; said MPU fetches multiple sequential instructions from said global memory unit in parallel, and said global memory unit supplies said multiple sequential instructions to said MPU during a single memory cycle. Official Notice is taken on this limitation. A person of ordinary skill in the art at the time the invention was made would have recognized that increasing the number of instructions fetched in a single cycle improves processor efficiency, since it decreases the amount of time needed to fetch instructions.

34. Referring to claim 50, Miller in view of Hanafi has not taught the microprocessor system of claim 45, wherein: said MPU further comprises an arithmetic logic unit (ALU) that is used for data operations and for branch address calculations. Official Notice is taken on this limitation. A person of ordinary skill in the art at the time the invention was made would have recognized that executing data operations and branch address calculations increases compatibility, Since more instructions can be executed.

35. Claims 51-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Hanafi as applied to claim 45 above, and further in view of Moore et al., U.S. Patent Number 5,070,451 (herein referred to as Moore).

36. Referring to claim 51, Moore has not taught the microprocessor system of claim 45, wherein: said MPU further comprises an arithmetic logic unit (ALU), and a first push down stack with a top item register and a next item register, connected to provide inputs to said ALU, an output of said ALU being connected to said top item register. Moore has taught a system with multiple push down stacks with registers storing the top item and next item (Moore column 2, line 29 to column 3, line 27; Figure 1; Figure 6; Figure 8; and Figure 9). A person of ordinary

skill in the art at the time the invention was made would have recognized, and as taught by Moore, that the stacks are faster and can be simultaneously accessed (Moore, column 5, lines 13-21), thereby decreasing the amount of time needed to access data in the stacks. Therefore, it would have Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the stacks and stack registers of Moore in the device of Miller to decrease the amount of time used to access data in the stacks.

37. Referring to claim 52, Miller in view of Hanafi and in further view of Moore has taught the microprocessor system of claim 45, wherein: said MPU comprises a zero-operand dual-stack architecture (Moore column 2, line 29 to column 3, line 27; Figure 1; Figure 6; Figure 8; and Figure 9).

38. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Hanafi in view of Moore as applied to claim 52 above, and further in view of Official Notice. Miller in view of Moore has not taught the microprocessor system of claim 52, wherein: said dual-stack architecture is cached on chip and automatically spills to and refills from external memory. Official Notice is taken on this limitation. A person of ordinary skill in the art at the time the invention was made would have recognized that, when a stack fills, overflow needs to spill over to somewhere to preserve the data.

39. Claims 81-82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Hanafi as applied to claim 45 above, and further in view of Hirata et al., U.S. Patent Number 5,430,851 (herein referred to as Hirata).

40. Referring to claim 81, Miller in view of Hanafi has not taught the microprocessor system of claim 45, wherein:

a. said MPU is operative to execute a first instruction stream; and

b. said IOP is operative to execute a second instruction stream different than said first instruction stream executed by said MPU.

41. Hirata has taught

a. an execution unit is operative to execute a first instruction stream (Hirata Figure 2(a)); and

b. a load/store unit is operative to execute a second instruction stream different than said first instruction stream executed by said MPU (Hirata Figure 2(a)).

42. A person of ordinary skill in the art at the time the invention was made, and as taught by Hirata, would have recognized that executing multiple instruction streams in parallel increases resource utilization efficiency and increases execution speed (Hirata column 1, lines 10-22). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hirata's parallel execution of multiple instruction streams in the device of Miller in view Hanafi to increase resource utilization efficiency and increase execution speed.

43. Referring to claim 82, Miller in view of Hanafi and in further view of Hirata has taught the microprocessor system of claim 81, wherein: said IOP executes said second instruction stream to cause data to be transferred (Hirata Figure 2(a)).

Conclusion

44. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

45. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183

10 November 2010